REMARKS

The application contains claims 1-26. Claims 16-22 have been cancelled and claims 23-26 have been added. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

Interview Summary

The substance of the interview is reported in the following remarks. The Examiner reserved judgment at the interview but agreed that the instant amendments were likely to overcome the outstanding rejections.

CLAIMS 1-6 AND 10-15 DEFINE OVER FRIENDLY

Claims 1-4 and 10-13 stand rejected as anticipated by Friendly. Claim 1 has been amended to recite:

> an instruction processing system in communication with the instruction cache, having a power control input coupled to the hit/miss output of the UOP cache.

Friendly does not teach or suggest this subject matter. For example, Friendly contains no disclosure regarding power control whatsoever. Accordingly, claims 1-4 define over this art.

Claim 10 also has been amended. It now recites:

> wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to unpower the data fetch unit selectively.

Again, Friendly has no disclosure regarding power control. Claims 10-13 are allowable as well.

CLAIMS 7-9 DEFINE OVER SHEPPARD

Claims 7-9 stand rejected as anticipated by Sheppard. Claim 7 has been amended to recite that the delay element has an input coupled to an output of the cache lookup unit and an output coupled to an input of the data fetch unit. Claim 7 further recites that the output of the delay element is a power control input to the data fetch unit. Sheppard discloses no such structure. The Office Action has interpreted the cache lookup element to read on Sheppard's

address RAM 60, 110 (FIGS. 3 and 6 respectively). Even if this analysis were correct, Sheppard's delay element 64 clearly does not take its input from the output of the address RAM. Claims 7-9, therefore define over the art.

New claims 23-26 depend from claim 7 and recite additional features that distinguish over the cited art. Claim 23 recites that the delay element synchronizes operation of the data fetch unit to a timing scheme of an external device. Claim 24 recites that the delay element is a multi-cycle delay element. Claim 25 recites that the delay element responds to a miss indicator from the cache lookup unit. Claim 26 recites that the cache is an element of a multi-cache system. Sheppard discloses none of these features. Accordingly, dependent claims 23-26 are independently allowable over this art.

Claim 9 has been amended to address the claim objections noted in paragraph 8 of the Office Action.

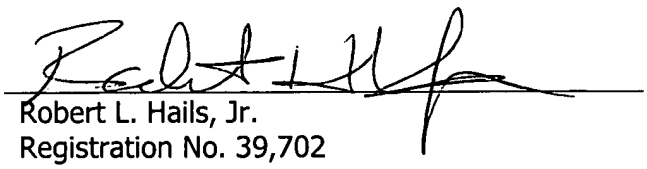
CONCLUSION

All claims are allowable over the cited art. Applicants respectfully request allowance of the application.

The Office is authorized to charge any fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

Date: May 10, 2004



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